## REMARKS

An excess claim fee payment letter is submitted herewith for four (4) excess total claims.

Claims 1, 3-9, and 11-26 are presently pending in the application. Claims 1, 3, 5-9, 11, and 13-16 have been amended to more particularly define the invention. Claims 19-26 have been added to assure Applicant the degree of protection to which his invention entitles him. Claims 2 and 10 have been cancelled in the interest of expediting prosecution.

The indication that claims 17-18 have been allowed is acknowledged with appreciation. New claims 19-26 are dependent from claims 17 and 18, and so are also allowable.

Claim 11 was rejected under 35 U.S.C. 112, second paragraph due to an editorial error. This has been corrected, and so this rejection is overcome.

Claims 1, 3, 9 and 11 were rejected under 35 U.S.C. §102(b) as being anticipated by Yamaguchi, et al., EP 1070980A1. Claims 2 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al. in view of Ikeda, JP No. 02150819. These rejections are respectfully traversed.

The claimed invention is directed to a voltage generating apparatus. In an exemplary embodiment, illustratively set forth in claim 1, the voltage generating apparatus includes an input terminal; an output terminal; a first offset voltage generating element connected to the input terminal; a slow discharging amplifier having an input, connected to the input terminal to receive input voltage therefrom, and having an output; a rapid charging amplifier having an input, connected to the first offset voltage generating element so that the input voltage applied

to the slow discharging amplifier is higher than an input voltage applied to the rapid charging amplifier, and having an output; and a current suppressing resistor coupling the output of the slow discharging amplifier to the output of the rapid charging amplifier. The output of one of the slow discharging amplifier and the rapid charging amplifier is connected directly to the output terminal.

In another exemplary embodiment, illustratively set forth in claim 9, the voltage generating apparatus includes an input terminal; an output terminal; a first offset voltage generating element connected to the input terminal; a rapid discharging amplifier having an input, connected to the input terminal to receive input voltage therefrom, and having an output; a slow charging amplifier having an input, connected to the first offset voltage generating element so that the input voltage applied to the rapid discharging amplifier is higher than the input voltage applied to the slow charging amplifier, and having an output; and a current suppressing resistor coupling the output of the rapid discharging amplifier to the output of the slow charging amplifier. The output of one of the rapid discharging amplifier and the slow charging amplifier is connected directly to the output terminal.

As to independent claim 1, Figure 6 of Yamaguchi, et al. discloses a voltage generating apparatus including an input terminal, an output terminal, a slow discharging amplifier connected between the input terminal and the output terminal, a rapid charging amplifier connected between the input terminal and the output terminal, an offset voltage generating element connected between the input terminal and one of the slow discharging amplifier and the rapid charging amplifier, so that the input voltage applied to the slow discharging amplifier is higher than the input voltage applied to the rapid charging amplifier.

(The Office Action designates terminal +N in Figure 6 of Yamaguchi as the input terminal. However, rapid charging amplifier 602, 605 is not connected between terminal +N and the output terminal. On the other hand, it is noted that line VDD in Yamaguchi's Figure 6 may be interpreted to fit the description of the input terminal, just as may line VLCD in Figures 15 and 16 of the present application.)

As to independent claim 9, Figure 5 of Yamaguchi, et al. discloses a voltage generating apparatus including an input terminal, an output terminal, a rapid discharging amplifier connected between the input terminal and the output terminal, a slow charging amplifier connected between the input terminal and the output terminal, an offset voltage generating element connected between the input terminal and one of the rapid discharging amplifier and the slow charging amplifier, so that the input voltage applied to the rapid discharging amplifier is higher than the input voltage applied to the slow charging amplifier. (In like manner, the Office Action designates terminal +N in Figure 5 of Yamaguchi as the input terminal. However, slow charging amplifier 502, 505 is not connected between terminal +N and the output terminal. On the other hand, it is noted that line VDD in Yamaguchi's Figure 5 may be interpreted to fit the description of the input terminal, just as may line VLCD in Figures 15 and 16 of the present application.)

As recognized in the Office Action, Yamaguchi does not show or suggest a resistor connected between the slow discharging amplifier and the output terminal (original claim 2) or between the slow charging amplifier and the output terminal (original claim 10). The Office Action contends that Ikeda's Figures 8-11 show this. This contention is traversed. Ikeda only has Figures 1-7; Ikeda has no Figures 8-11.

Ikeda shows a voltage providing circuit in which operational amplifiers OP1-OP4 have their inputs connected to a voltage divider circuit and which have respective resistors R8-R11 coupling their outputs to respective output terminals V1-V4. Each operational amplifier has a resistor connected to its output.

Independent claims 1 and 9 include a current limiting resistor coupling the outputs of the discharging amplifier and the charging amplifier. As set forth in the specification at, for example, page 13, lines 16-18 and page 15, lines 11-13, this current limiting resistor suppresses an ON-ON current when the output transistors of the discharging amplifier and the charging amplifier are both turned on.

Ikeda does not show or suggest a current limiting resistor coupling the outputs of the discharging amplifier and the charging amplifier. If anything, Ikeda leads away from the subject matter of claims 1 and 9 by teaching a transistor in the output of each amplifier.

Further, independent claims 1 and 9 recite that the output of one of the discharging amplifier and the charging amplifier is connected directly to the output terminal. In Ikeda's circuit, each operational amplifier has a resistor connecting its output to the circuit output terminal.

It is accordingly submitted that claims 1, 3-9, and 11-16 distinguish patentably from the references and are allowable.

A minor error has been corrected in the disclosure.

In view of the foregoing, Applicant submits that claims 1, 3-9, and 11-28, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would

be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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